Phase noise analysis of a tail-current shaping technique employed on a BiCMOS voltage-controlled oscillator

by Wynand Lambrechts and Prof Saurabh Sinha

Several techniques exist to improve phase noise performance in voltage-controlled oscillators (VCOs). These techniques range from VCO topology considerations, inductor dimensioning and placement for improved quality factor (Q-factor), semiconductor process parameter considerations, and reducing low-frequency tail-current noise sources. The latter option is employed to study the overall effect on VCO phase noise performance, as it has been recognised that the tail transistor may have a large impact on the generation of phase noise, often being the largest contributor.

Tail-current noise suppression in radio frequency (RF) BiCMOS VCOs prevents the low-frequency tail-current noise from being converted into phase noise during normal operation of the oscillator. The tail current is made large when the oscillator output voltage reaches its maximum or minimum value and when the sensitivity of the output phase to injected noise is the smallest. The tail current is made small during the zero crossings of the output voltage when the noise sensitivity is large. No additional power is added to the system, ensuring low power operation at low noise levels. Tail-current shaping techniques reduce phase noise with three separate, but simultaneous mechanisms. The increased oscillation amplitude, narrower drain current pulses, and finally the shunt capacitor that acts as a noise filter for the tail current, all contribute to lowering the phase noise.

Silicon Germanium (SiGe) BiCMOS processes, implemented with heterojunction bipolar transistors (HBTs), offer remarkable high-frequency performance (with peak currently at 350 GHz) without large expense of noise (through trapping of hot carriers in the isolation between the emitter and extrinsic base) performance, with low-cost implementation possible and compatibility with very large-scale integration (VLSI) processes. Doping of the Silicon (Si) transistor base-layer with a Germanium-graded composition lowers the thermal conductivity of the transistor and increases electron mobility, which results in faster switching speeds compared to Si processes.

The VCO was implemented using the 0.35 µm BiCMOS (thick metal) process provided by Austriamicrosystems (AMS).

To achieve a low phase noise VCO, several considerations influence the overall operation and phase noise characteristics of the VCO. The initial VCO should operate at respectable phase noise levels, and improvements to the phase noise should give the VCO an edge over existing works, bearing in mind the technology used for integration. Some of these considerations include the topology of the VCO, inductor geometry and quality, design process, current source topology, and finally the method used to improve phase noise performance.

For the design process, some comparable oscillator specifications have been achieved using CMOS, BiCMOS and InGaAs/GaAs technologies. It is important to weigh performance versus cost-effectiveness and ease of implementation as trade-offs when choosing the process technology. Therefore, SiGe BiCMOS was chosen as the preferred process for implementation. An advantage of this process, compared to GaAs, is its compatibility with silicon VLSI processes and scalability to higher current densities.

Considering the inductor geometry, when designing a low phase noise RF VCO, an inductor with a good quality factor with minimum additive noise is critical. Spiral inductors are commonly used for on-chip integration. For the tank circuit, a standard spiral inductor was implemented. For the tail-current filter, a spiral inductor with larger inductance but lower Q-factor was chosen. The Q-factor does not influence overall circuit performance and the increased inductance has an advantage of creating a higher impedance path between the tail-current and switching transistors to limit the up-conversion of low-frequency noise.

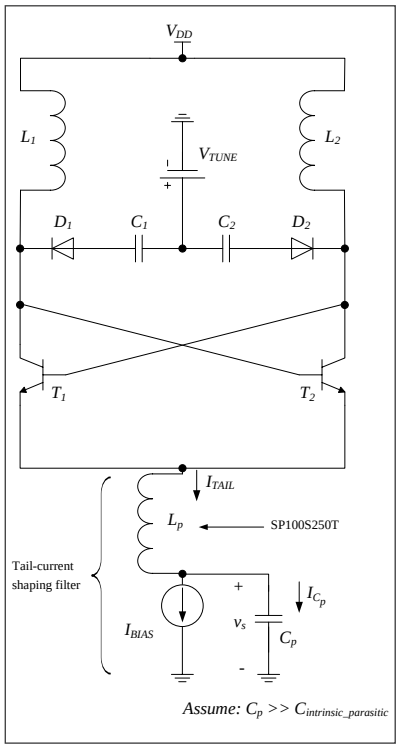
Topology considerations showed that LC oscillators display the most attractive characteristics for high-frequency, low phase noise designs. These oscillators consist of a tank circuit with a quality factor that can

be improved by improving the Q-factor of the inductor. Phase noise ratings of between -110 dBc/Hz and -130 dBc/Hz at an offset of 1 MHz from their respective 5 GHz carriers have been reported.

For the current source, a Widlar current mirror presents a stable current as any changes in output current are countered with a decrease in the gate-source voltage of the driver transistor.

Tail-current shaping

A tail-current shaping circuit presents a high impedance path that circulates odd harmonics in a differential path, while even harmonics flow in a common-mode path through the switching transistors towards the ground. This entails the employment of a filtering technique to suppress low noise modulation of the dominant even (second) harmonic where device noise is up-converted to noise. Subsequent harmonics are assumed to be minute and negligible. An important factor to consider is that the filter capacitor may be detrimental to the overall phase noise performance of the current-source driver as the transistor enters the triode region and therefore this transistor must ideally be kept in the active region. The tail-current filtering technique is shown in Figure 1.



→ *Figure 1. Tail-current shaping technique employed to LC VCO.*

A capacitor (C_p) in parallel with the current source, as seen in Figure 1, adds a path that the current may follow during operation, as shown below (assuming that it is much larger than the intrinsic gate-drain (C_{GD}) and base capacitance (C_π).

$$I_{TAIL} = I_{BIAS} - I_{C_p} \quad (1)$$

The capacitor is sized so that most of the current generated at (2) is grounded. The voltage across the capacitor (v_s) is given by the following formula:

$$v_s = A_s \cos(4\pi f_0 t - \theta) \quad (2)$$

where A_s is the voltage amplitude at this point, and θ is the phase delay between the output signal and the signal measured at the common emitters of the switching transistors. The current through the capacitor is as follows:

$$i_c = C_p \frac{dv_s}{dt} = -4\pi A_s f_0 C_p \sin(4\pi f_0 t - \theta) \quad (3)$$

Therefore, the maximum current through the capacitor from (3) is $-4\pi A_s f_0 C_p$. If this value is set to I_{BIAS}, a minimum current I_{TAIL} is achieved at $2f_0$. Thus,

$$C_p = \frac{21_{BIAS}}{4\pi A_s f_0} \quad (4)$$

where the 21_{BIAS} current reflects the peak-to-peak value, the dominant part of the current at the distorted second harmonic will flow through the capacitor, towards ground during $2f_0$. To ensure that the current at the fundamental frequency component, where most of the power lies, does not pass through the capacitor freely, an inductor (L_p) is placed between the current source and the differential pair, as depicted in Figure 1. The inductor and capacitor creates a band-pass inductor-capacitor (LC) filter configuration. The inductor also increases the impedance path between the switching transistors and current source to avoid noise from the low frequency currents to be up-converted to phase noise in the oscillator.

Simulation results

Simulation results confirm that tail-current shaping has enhanced the phase noise performance of an LC BiCMOS VCO, as summarised in Table 1.

Offset frequency	10 kHz	100 kHz	1 MHz
Without tail-current shaping	-57.61	-83.7	-105.3
With tail-current shaping	-64.9	-88.1	-108.6
Improve-ment	7.3	4.4	3.3

→ *Table 1[1]. Phase noise simulation results.*

The simulated results for the VCO with the tail-current shaping filter employed is depicted in Figure 2, where the vertical axis represents the phase noise in dBc/Hz and the horizontal axis is the relative offset frequency from the 5 GHz carrier.

The VCO was implemented on-chip (see Figure 3) to relate the measured results (as seen in Figure 4) with the simulated results. Figure 3 indicates the prototyped circuit used for measurements, as well as the relative size that the inductor occupies on die.

[1] All tabulated values represent the phase noise rating in dBc/Hz at a 1 MHz offset from the 5 GHz carrier frequency.

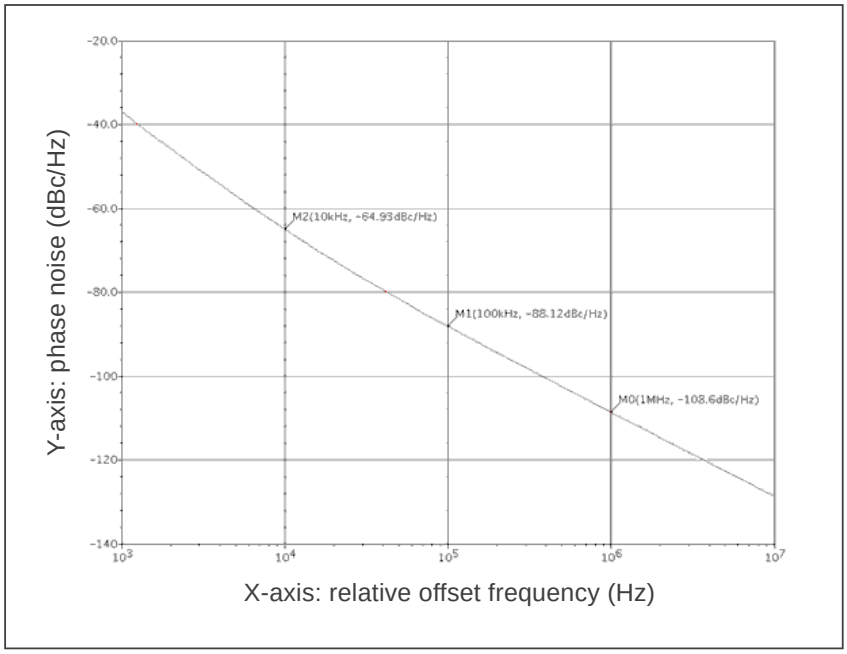


Figure 2. Simulation results of VCO with tail-current shaping.

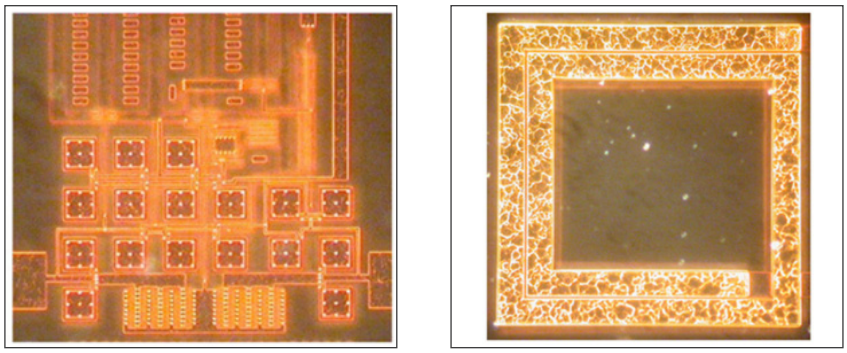


Figure 3. Prototyped circuit and inductor.

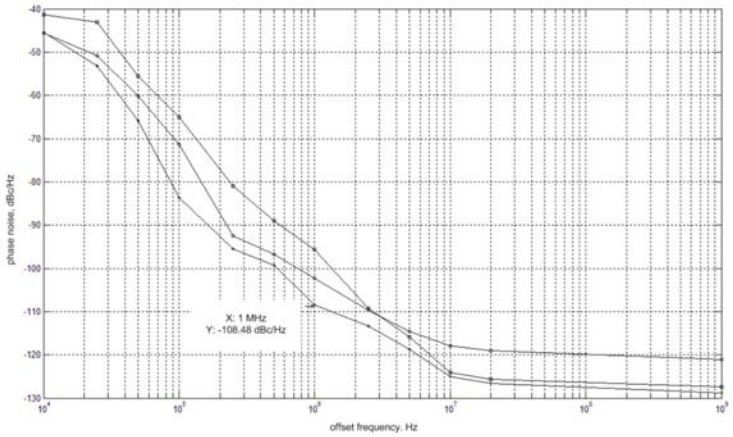


Figure 4. Measured phase noise of prototyped VCOs.

However, an error was encountered during the layout process of the VCO, and the relative phase noise improvement between separate VCOs could not be measured. The measured results can only serve as proof that the simulated phase noise correlates with the prototype phase noise of around -108.5 dBc/Hz at a 1 MHz offset from the 5 GHz carrier frequency.

Simulation results provided a 3.3 dBc/Hz improvement from -105.3 dBc/Hz to -108.6 dBc/Hz at a 1 MHz offset frequency from the 5 GHz carrier when employing tail-current shaping. The relatively small improvement in VCO phase noise performance translates in higher modulation accuracy when used in a transceiver. This increase can therefore be regarded as significant. The power consumption of the simulated VCO is around 6 mW and 4.1 mW for the measured prototype. The circuitry occupies 2.1 mm^2 of the die area.

The simulation results confirm a 3.3 dBc/Hz phase noise improvement at 1 MHz offset from the 5 GHz carrier when employing tail-current shaping. The LC VCO was designed in a technology that not only contains metal-oxide-semiconductor field effect transistors (MOSFETs), but is combined with the speed and low noise of SiGe heterojunction bipolar transistors (HBTs). Tail-current shaping can be expanded for other configurations (and ring oscillators), which could serve as a good basis for future work. If this application proves viable in a number of different scenarios apart from experimental results obtained here, it could be used as a standard implementation to provide a guaranteed improvement on phase noise without the use of any expensive, process-altering techniques.

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Student research earns award at peer-reviewed international conference

The research paper of Wynand Lambrechts, a student in the Department of Electrical, Electronic and Computer Engineering at the University of Pretoria, was awarded the Best Paper Award in the Student Paper category at the 33rd International Semiconductor Conference (CAS 2010), which was held in Sinaia, Romania, in October 2010.

This conference was technically co-sponsored by the Institute of Electrical and Electronics Engineers (IEEE). Wynand's travels were funded as part of a National Research Foundation (NRF) grant. His master's research, conducted under the supervision of Prof Saurabh Sinha, involved a phase noise analysis of a tail-current shaping technique employed on a BiCMOS voltage-controlled oscillator.

As part of his studies, Wynand also spent two months at the non-linear radio frequency (RF) laboratory at Ohio State University (OSU) in the USA, which is a top international laboratory in this field.

This visit provided him the opportunity to expand his knowledge of microelectronic engineering to the point where it was possible to improve his skills. It enabled him to focus future research on making a unique or novel contribution. The aim of this visit was specifically to spend time at the non-linear RF laboratory at OSU and to perform measurements on a prototype integrated circuit (IC) using equipment not available in South Africa, and to get an idea of the work being done outside South Africa in his specific field of research.